

CLAIMS

1. (Original) A memory module comprising:
a redrive circuit to receive a signal from a first point-to-point link and redrive the signal on a second point-to-point link;
a memory device; and
a data accumulator coupled between the redrive circuit and the memory device.
2. (Original) A memory module according to claim 1 wherein the point-to-point links comprise unidirectional links.
3. (Original) A memory module according to claim 1 wherein the data accumulator comprises a FIFO structure.
4. (Original) A memory module according to claim 1 further comprising a second redrive circuit to receive a second signal from a third point-to-point link and redrive the second signal on a fourth point-to-point link.
5. (Original) A memory module according to claim 4 wherein the memory device is coupled to the second redrive circuit.
6. (Original) A memory module according to claim 5 further comprising a second data accumulator coupled between the memory device and the second redrive circuit.
7. (Original) A memory module according to claim 1 wherein the memory device has a burst bandwidth that is greater than the bandwidth of the redrive circuit.
8. (Original) A memory module according to claim 1 wherein the data accumulator is constructed and arranged to accumulate data from the redrive circuit.
9. (Original) A memory module according to claim 1 wherein the data accumulator is constructed and arranged to accumulate data to the redrive circuit.

10. (Original) A memory buffer comprising:
a redrive circuit to receive a signal from a first point-to-point link and redrive the signal on a second point-to-point link; and
a memory interface coupled to the redrive circuit, wherein the memory interface comprises a data accumulator.
11. (Original) A memory buffer according to claim 10 wherein the point-to-point links comprise unidirectional links.
12. (Original) A memory buffer according to claim 10 wherein the data accumulator comprises a FIFO structure.
13. (Original) A memory buffer according to claim 10 further comprising a second redrive circuit to receive a second signal from a third point-to-point link and redrive the second signal on a fourth point-to-point link.
14. (Original) A memory buffer according to claim 13 further comprising a second data accumulator coupled between the memory interface and the second redrive circuit.
15. (Original) A memory system comprising:
a memory controller;
a memory agent having a redrive circuit; and
a first point-to-point link arranged to transmit a signal from the controller to the redrive circuit of the memory agent;
wherein the memory agent comprises a data accumulator coupled to the redrive circuit.
16. (Original) A memory system according to claim 15 wherein the point-to-point links comprise unidirectional links.
17. (Original) A memory system according to claim 15 wherein the data accumulator comprises a FIFO structure.

18. (Canceled)
19. (Original) A memory system according to claim 15 further comprising a second point-to-point link arranged to transmit a signal from the memory agent to the controller.
20. (Original) A memory system according to claim 15 wherein the memory agent further comprises a second redrive circuit.
21. (Original) A memory system according to claim 18 wherein the memory agent further comprises a second data accumulator coupled to the second redrive circuit.
22. (Original) A method for operating a memory agent comprising:
receiving a first signal on a first point-to-point link;
redriving the first signal on a second point-to-point link;
accumulating write data from the first signal; and
delivering the write data to a memory device.
23. (Original) A memory system according to claim 22 wherein the point-to-point links comprise unidirectional links.
24. (Original) A method according to claim 22 wherein accumulating and delivering the write data comprises accumulating and delivering the write data in a FIFO sequence.
25. (Original) A method according to claim 22 further comprising:
receiving a second signal on a third point-to-point link; and
redriving the second signal on a fourth point-to-point link.
26. (Original) A method according to claim 22 further comprising:
accumulating read data from a memory device; and
transmitting the read data as the second signal.